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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,701	11/26/2003	Michael J. Berman	03-1494	7831
24319 75	590 10/28/2005		EXAM	INER
LSI LOGIC CORPORATION 1621 BARBER LANE			KOBERT, RUSSELL MARC	
MS: D-106			ART UNIT	PAPER NUMBER
MILPITAS, CA 95035			2829	

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)				
	10/723,701	BERMAN ET AL.				
Office Action Summary	Examiner	Art Unit				
	Russell M. Kobert	2829				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on <i>08 Au</i>	<u>ugust 2005</u> .					
2a)⊠ This action is FINAL . 2b)☐ This	action is non-final.					
3) Since this application is in condition for allowar	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice under E	x parte Quayle, 1935 C.D. 11, 45	53 O.G. 213.				
Disposition of Claims						
4) ☐ Claim(s) 1-18 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-18 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9) The specification is objected to by the Examiner. 10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119		•				
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:					

1. Applicant's arguments filed 8 August 2005 have been fully considered but they are not persuasive.

Applicants argue that Hirao is non-analogous art because the instant application is used in a semiconductor wafer electroplating process whereas Hirao only relates to probe cards for performing a wafer test and chip test of semiconductor devices. Applicants further argue that Hirao does not disclose or suggest that the probe card checker both sends and receives test signals and measures the resistances.

These arguments are not persuasive because a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In the instant invention, Applicants' only state that the device is used in a semiconductor electroplating process however no structure that positively recites is described in the body of the claim 1. Applicants are further reminded that such a recitation has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

In regard to the measurement of resistances, it is a scientific principle of electronics that a resistance measurement requires a known current that is carried through a load and returns from the load to produce a voltage drop across the unknown load to be measured and using the formula for resistance measurement, R=V/I, one having ordinary skill in the art would have known that the technique disclosed by Applicants is a well know phenomenon.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirao (6788082).

Hirao anticipates (in each of the combined figures) a device and method for measuring resistances associated with electrical contacts of a contact ring used in a semiconductor wafer electroplating process, comprising:

a substrate (102) which is *configured* such that the substrate is *mountable* in the contact ring;

a conductive pattern on said substrate (inherent to the Metal Plate 102 because there would have to exist some form of conduction between the Probe Card Checker 101 and each individual probe pin $[P_1 - P_N]$ on the Metal Plate), said conductive pattern electrically contactable with the electrical contacts of the contact ring (see circular ring located at center of probe card 4); and

resistance measurement circuitry connected to said conductive pattern, said resistance measurement circuitry *configured to* not only send test signals to said conductive pattern, but also *configured to* receive signals from the conductive pattern and measure the resistances associated with the electrical contacts of the contact ring (col 5, ln 36 - col 6, ln 2); as recited in claims 1 and 12.

As to claim 2, Hirao anticipates the substrate is at least one of a silicon substrate and a metal substrate (Metal Plate 102).

As to claims 3 and 13, having the resistance measurement circuitry configured to communicate signals to an external device, the signals relating to resistances to the electrical contacts of the contact ring is considered inherent to the operation of the Probe Card Checker 101.

As to claims 4-11 and 14-18 having a battery to power the resistance measurement circuitry, having input/output circuitry connected to the conductive pattern, having multiplexer circuitry connected to the conductive pattern, resistance determination circuitry and the remaining claimed components and operational characteristics is considered to be within the scope of Hirao.

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4. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Russell Kobert whose telephone number is (571) 272-

1963.

The Examiner's Supervisor, Nestor R. Ramirez, can be reached at (571) 272-

2034.

For an automated menu of Tech Center 2800 phone numbers call (571) 272-

2800.

Russell M. Kobert

Patent Examiner

Group Art Unit 2829

October 24, 2005

VINH NGUYEN PRIMARY EXAMINER

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10/27/05